

DESCRIPTION

The SW7125D is a Low Noise Amplifier designed for Global Navigation Satellite Systems (GNSS) as GPS, GLONASS, Galileo and Compass. The SW7125D requires only one external input matching inductor, reduces assembly complexity and the PCB area, enabling a cost-effective solution.

The SW7125D achieves ultra-low noise figure, high gain, over a wide range of supply voltages from 1.5V up to 3.6V. All these features make SW7125D an excellent choice for GNSS LNA as it improves sensitivity with low noise figure and high gain, provide better immunity against out-of-band jammer signals with high linearity, reduces filtering requirement of preceding stage and hence reduces the overall cost of the GNSS receiver.

The SW7125D is available in a small lead-free, RoHS-Compliant, 1.5mm x 1.0mm x 0.75mm 6-pin DFN package.

FEATURES

- **Ultra-low noise figure(NF)=0.65dB;**
- **High power gain=18.0dB;**
- **Low supply current: 6.9mA;**
- **High input 1dB-compression point= -8dBm;**
- **Requires only one input matching inductor;**
- RF output internally matched to 50 ohms;
- Supply voltage: 1.5V to 3.6V;
- Operating frequencies: 1550~1615MHz;
- DFN-6L package: 1.5mmX1.0mmX0.75mm;
- 3kV HBM ESD protection (including RFIN and RFOUT pin).

APPLICATIONS

- Smart phones, Tablet PCs;
- Personal Navigation Devices;
- Complete GPS/BDS chipset modules;
- Theft protection (laptop, ATM);
- Smart watch and other mobile devices.

PIN CONFIGURATION AND MARKING

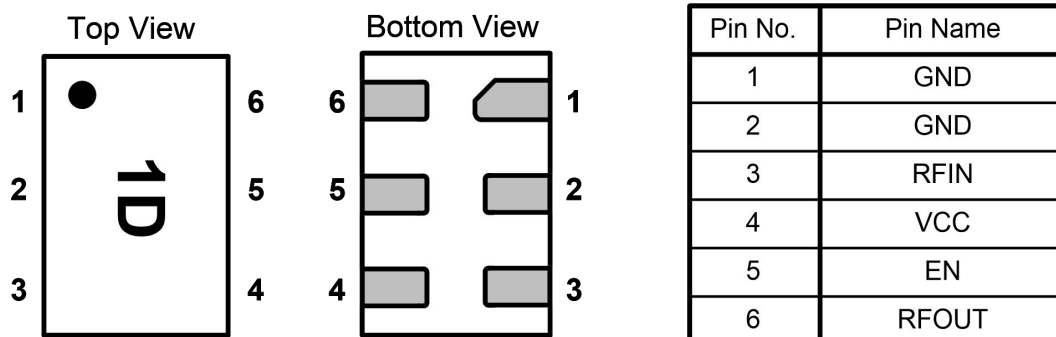


Figure 2. SW7125D Pin Configuration and Marking

TYPICAL APPLICATION

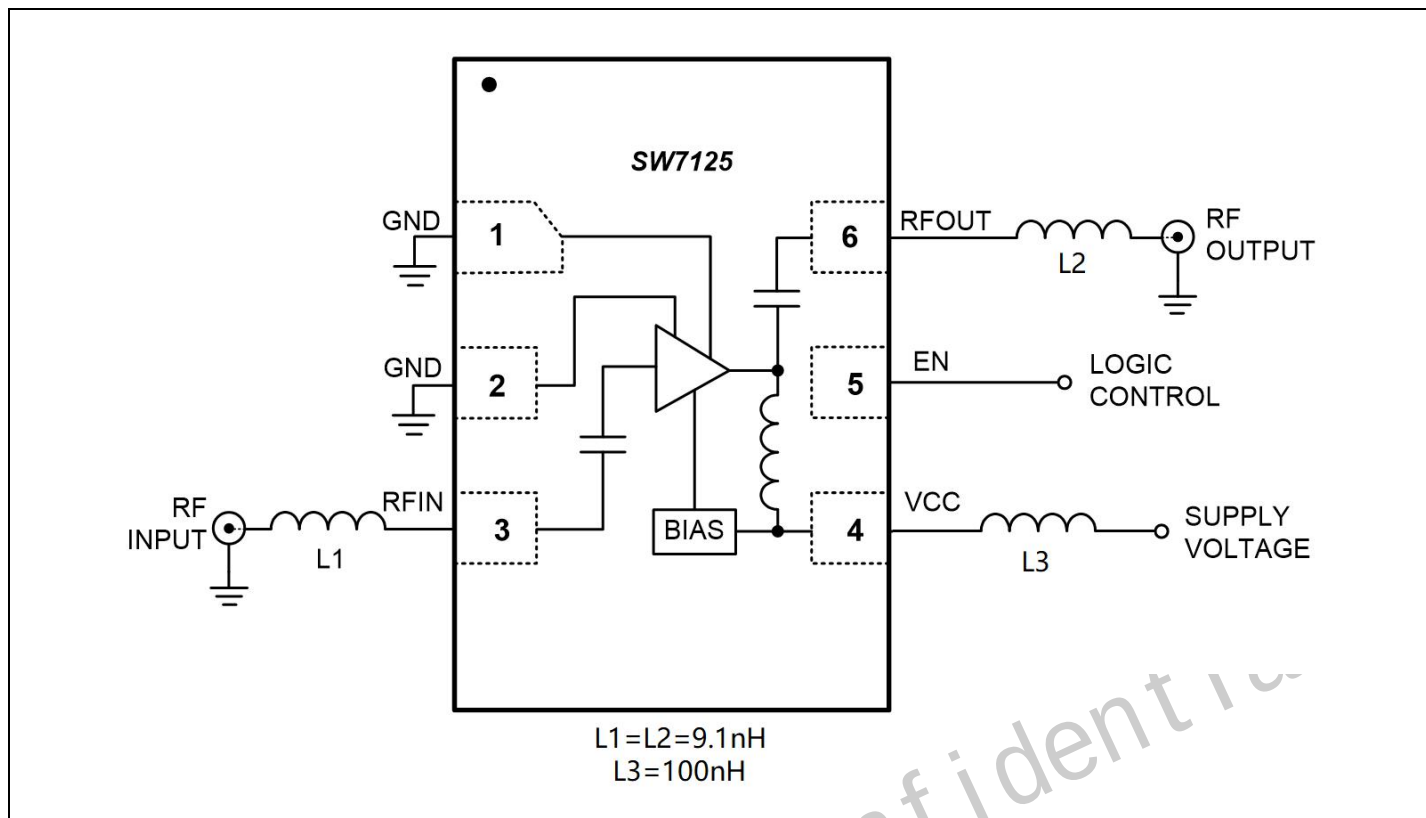


Figure 3. Application Schematic SW7125D

For a list of components see [Table4](#) and [Table5](#)

ORDER INFORMATION

Table 1. Order Information

Part Number	Temperature	Package	RoHS	Mark	SPQ
SW7125D	-40°C ~ 85°C	1.5mm x 1.0 mm x 0.75mm DFN-6L	Yes	1D	Tape and Reel 3000 pcs/Reel

SW7125□□□
 R : Tape&Reel
 DN: DFN

ABSOLUTE MAXIMUM RATINGS

Table 2. Limiting Values

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Supply Voltage at pin VCC	V _{CC}	-0.3	-	5.0	V
Voltage at pin EN	V _{EN}	-0.3	-	5.0	V
Current into pin VCC	I _{CC}	-	-	30	mA
RF input power	P _{IN}	-	-	10	dBm
Package thermal resistance	θ _{JA}	-	148.2		°C/W
Junction temperature	T _J	-	-	150	°C
Storage temperature range	T _{STG}	-65	-	150	°C
Ambient temperature range	T _{amb}	-40	-	85	°C
Solder temperature(10s)		-	260	-	°C
ESD range					
HBM ¹⁾		±3000			V
MM ²⁾		±250			V
Latch-up					
Standard: JEDEC STANDARD NO.78DNOVEMBER 2011		+IT: +400 -IT: -400			mA mA

Note 1: HBM standard: MIL-STD-883H Method 3015.8.

Note 2: MM standard: JEDEC EIA/JESD22-A115.

ELECTRICAL CHARACTERISTICS

(SW7125D EVB¹⁾; $V_{CC}=1.5$ to $3.6V$, $T_A=-40\sim+85\text{ }^{\circ}C$, $f=1550MHz$ to $1615MHz$; Typical values are at $V_{CC}=2.8V$ and $T_{amb}=+25\text{ }^{\circ}C$, $f=1575.42MHz$, unless otherwise noted.)

Table 3. Electrical Characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
V_{CC}	Supply Voltage		1.5	-	3.6	V
I_{SD}	Shut-Down Current	EN=Low			1.0	μA
I_{CC}	Supply Current	EN=High		6.9		mA
V_{EN}	Digital Input-Logic High		0.80			V
V_{EN}	Digital Input-Logic Low			0.45		V
AC ELECTRICAL CHARACTERISTICS						
G_p	Power Gain			18.0		dB
RL_{in}	Input Return Loss			9.3		dB
ISL	Reverse Isolation			28.5		dB
RL_{out}	Output Return Loss			14.2		dB
NF	Noise Figure	$Z_s=50\text{ ohm}$; No jammer		0.65		dB
K_f	Stability factor	$f=20MHz\sim 10GHz$	1.0			
NF_j	Noise Figure with jammer	$P_{jam}=-20dBm$; $f_{jam}=850MHz$		TBD		dB
		$P_{jam}=-20dBm$; $f_{jam}=1850MHz$		TBD		dB
IP_{1dB}	Inband input 1dB-compression point	$f=1575.42MHz$;		-7.8		dBm
$IIP3_{oob}$	Out-of-band input 3 rd -order intercept point	$f_1=1712.7MHz$; $f_2=1850MHz$; $P_{in}=-20dBm$		TBD		dBm
$IIP3_{oob}$	Out-of-band input 3 rd -order intercept point	$f_1=1712.7MHz$; $f_2=1850MHz$; $P_{in}=-30dBm$		TBD		dBm
H2-input referred	LTE band-13 2 nd Harmonic	$f=787.76MHz$; $P_{in}=-25dBm$; $f_{H2}=1575.52MHz$		TBD		dBm
t_{on}	Turn-on time			2.2		μs
t_{off}	Turn-off time			1.7		μs

Note1: input matched to 50 ohms using a high quality-factor 9.1nH inductor.

APPLICATION INFORMATION

1.1 EN control

The SW7125D includes an internal switch to turn off the entire chip: apply logic high to EN to turn on, and a logic low to shut down.

1.2 List of components

1. The SW7125D requires only one external inductor for input matching. If the device/phone manufacturers implement very good power supply filtering on their boards, the bypass capacitor mentioned in this application circuit may be optional. With the capacitor, we can get better performance like a little higher gain etc. The value is optimized for the best gain, noise figure, return loss performance. Typical value of inductor is 9.1nH, capacitor is 1nF. For schematics see [Figure2](#).
2. The output of SW7125D is internally matched to 50 ohms and a DC blocking capacitor is integrated on-chip, thus no external component is required at the output.
3. The SW7125D should be placed close to the GPS antenna with the input-matching inductor. Use 50-ohm micro-strip lines to connect RF INPUT and RF OUTPUT. Bypass capacitor should be located close to the device. For long Vcc lines, it may be necessary to add more decoupling capacitors. Proper grounding of the GND pins is very important.

Table 4 lists the recommended inductor types and values;

Table 4: list of inductor

Part Number	Inductance	Q(min)	Q Test Frequency	Supplier	Size
Units	nH		MHz		
LQW15A	9.1	25	250	Murata	0402
SDWL1005C	9.1	24	250	Sunlord	0402
HQ1005C	9.1	22	250	Sunlord	0402

Table 5 lists the recommended capacitor types and values.

Table 5: list of capacitor

Part Number	Capacitance	Rated Voltage	Supplier	Size
Units	pF	V		
GRM155	1000	50	Murata	0402

PACKAGE INFORMATION

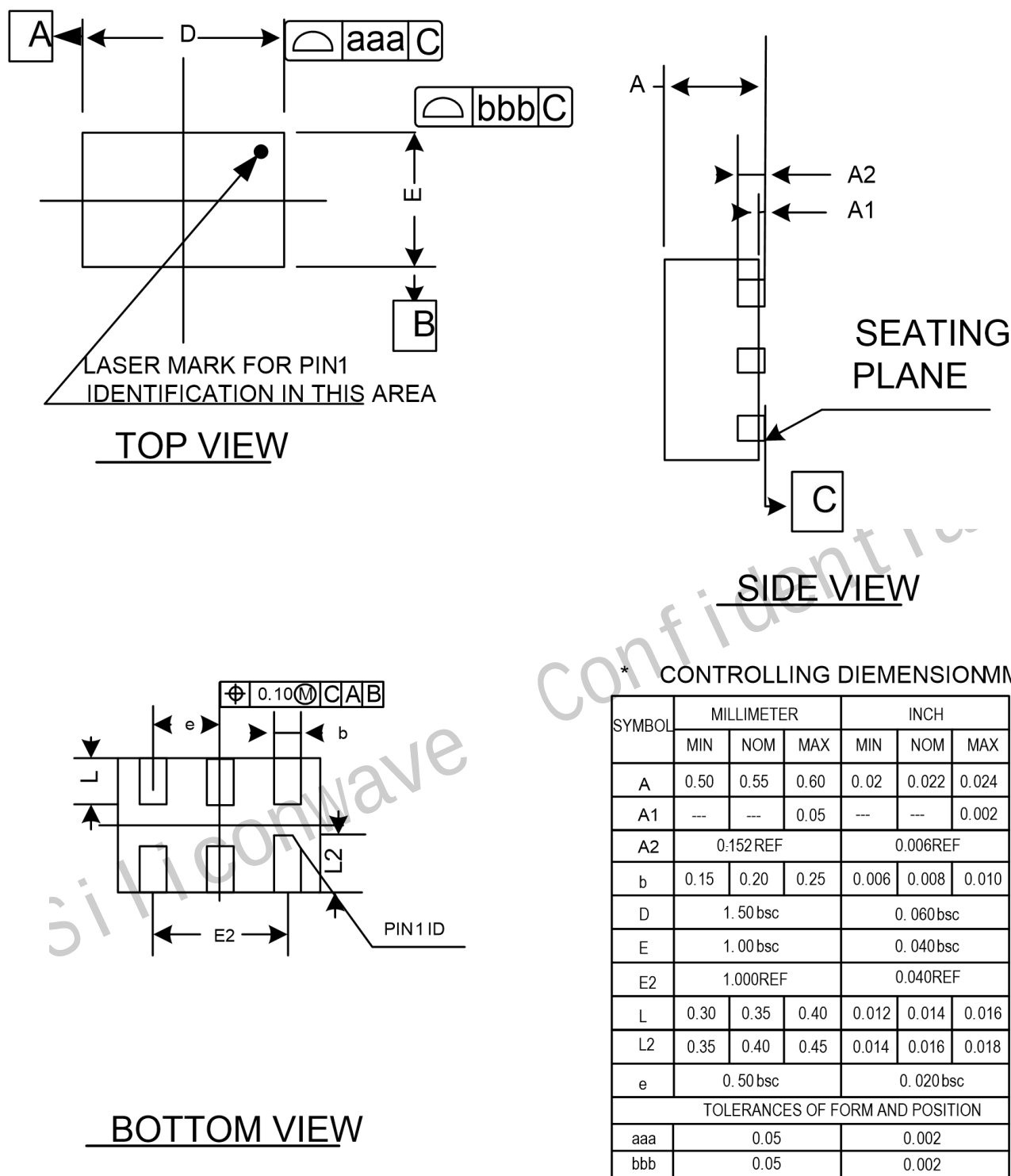
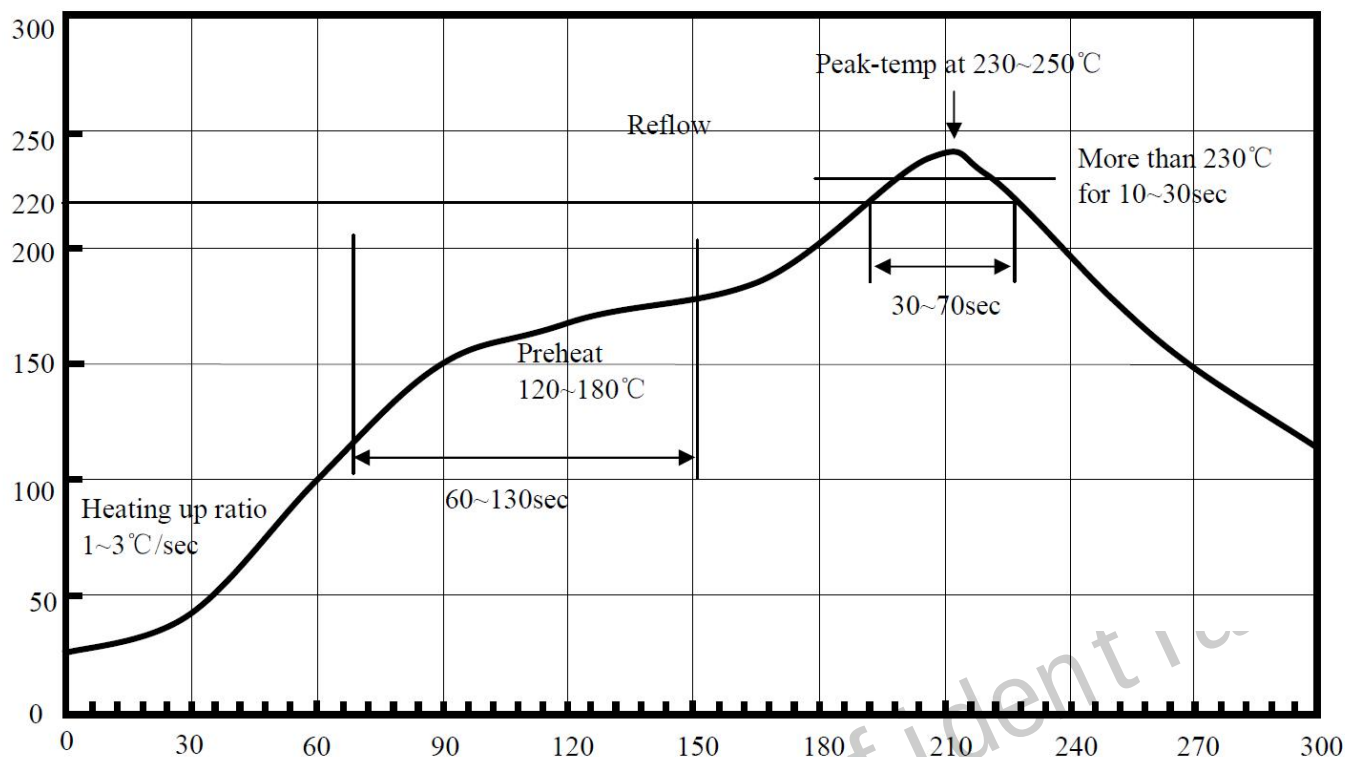


Figure 4. Package Outline

RECOMMENDED SOLDER TEMPERATURE



ROHS COMPLIANT

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.